UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,653	02/27/2002	Wilhelm Koenig	449122024500	9474

7590 05/04/2005

Kevin R. Spivak
Morrison & Foerster LLP
Suite 5500
2000 Pennsylvania Avenue, N.W.
Washington, DC 20006-1888

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,653	KOENIG ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004 and 27 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the applicant's amendments dated 11/24/2004 and 12/27/2004.

Claims 1 and 11 were amended.

Claims 1-11 are pending.

Response to Amendment

1. In view of the applicant's changes to the Specification and Drawings, the examiner withdraws the objections to said Specification and Drawings, and approves the changes.

2. In view of the applicant's amendments to Claims 1 and 11, the examiner withdraws the rejections of said claims under 35 USC 112 second paragraph for antecedent issues and also for indefiniteness of the claims.

Response to Arguments

3. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new grounds of rejection (see below).

Claim Rejections - 35 USC § 102

4. Claims 1, 3 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Volk et al., U.S. Patent No. 4792950.

As per Claims 1 and 11:

Volk et al. teaches a method and circuit for the detection of an interruption in a differential signal feed (see Abstract), comprising: a pair of input terminals (FIG.1 12, 14) receiving differential data signals (column 2 lines 11-13); and two inputs of a data comparator (FIG.1 70), connected to the input terminals, to generate data (FIG.1 CD), wherein the two input terminals are connected to respective comparators (FIG.1 62, 66), the comparators have an auxiliary voltage applied on the input side (FIG.1 REF V_1, V_2), and signals at outputs of the comparators (FIG.1 CA, CB) are evaluated such that an interruption of at least one of the signal feeds is detected (column 5 lines 49-67).

As per Claim 3:

Volk et al. further teaches the input circuit as claimed in claim 1, wherein the input terminals are connected via a resistor to a terminating potential (12 via 46 to Vcc, 14 via 48 to common).

Claim Rejections - 35 USC § 103

5. Claims 2, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al.; U.S. Patent No. 4792950 as applied to claim 1 above, and further in view of Barish et al., U.S. Patent No. 4967151.

As per Claim 2:

Volk et al. fails to teach the input circuit as claimed in claim 1, wherein the input circuit is arranged in an integrated circuit. But in the analogous art of Barish et al., this feature is disclosed in the Summary. And, column 3 lines 1-30, for example, cites an

advantage of providing shorts fault detection between the interconnect lines of differential circuits. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to provide the addition short fault checking to the circuitry of Volk in order to improve fault detecton.

As per Claim 6:

Barish et al. further teaches the input circuit as claimed in claim 2, wherein resistors are arranged in the integrated circuit (FIG.5). And in view of the motivation previously stated, the claim is rejected.

As per Claim 7:

Barish et al. fails to teach the input circuit as claimed in claim 2, wherein resistors are arranged outside the integrated circuit. But in the analogous art of Volk et al., FIG.1 teaches this feature. And in view of the motivation previously stated, the claim is rejected.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al., U.S. Patent No. 4792950 as applied to claim 3 above, and further in view of Ichie, U.S. Patent No. 5050187. Volk et al. fails to teach the input circuit as claimed in claim 3, wherein there is at least one current source, which is supplied to the auxiliary voltages at the resistors. But in an analogous art, Ichie does teach this feature (column 14 lines 23-43 and FIG.18 J1 or J2). And in Ichie (column 2 lines 27-34), an advantage is stated which provides stable transmissions over differential lines in the event of shorted or open lines. One with ordinary skill in the art at the time of the invention, motivated as

suggested, would find it obvious to include the current source teachings of Ichie in order to improve the performance of a communications system.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al., U.S. Patent No. 4792950 as applied to claim 1 above, and further in view of Phillips, U.S. Patent No. 3825682. Volk et al. fails to teach the input circuit as claimed in claim 1, wherein the auxiliary voltage is greater than the maximum input offset of the comparators and smaller than a minimum voltage swing of the data signal. But in an analogous art, Phillips does teach this feature in column 2 lines 19-47 and FIG.2. The advantage of this invention is stated in column 1 lines 48-67, where a circuit is provided which detects opens and shorts in the input lines. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to include the reference voltage teachings of Phillips in order to improve the performance of a differential receiver.

8. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al., U.S. Patent No. 4792950 as applied to claim 2 above, and further in view of Barish et al., U.S. Patent No. 4967151 as applied to Claim 7 above, and further in view of Ichie, U.S. Patent No. 5050187. Volk et al. and Barish et al. fail to further teach the input circuit as claimed in claim 7 with current sources and voltage. However, Ichie teaches the input circuit having two current sources (FIG.18 J1, J2), each connected to one of the input terminals (FIG.18 A, B) and to a supply potential (FIG.18 Vcc), and each of the

two current sources impresses a current which is lower than the currents flowing during normal operation (column 14 lines 25-43). And in view of the motivation previously stated, the claim is rejected.

9. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al., U.S. Patent No. 4792950 as applied to claim 1 above, and further in view of Sunter, U.S. Patent No. 6586921. Volk et al. fails to further teach the input circuit as claimed in claim 1, wherein the outputs of the comparators are respectively connected to a boundary scan cell of a boundary scan shift register. But in the analogous art of Sunter, this feature is taught in column 20 lines 54-67, column 21 lines 1-8, lines 49-54, and lines 61-63. And in column 4 lines 3-10, the invention provides special testing, such as input current leakage, using conventional low cost test protocol. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to add the boundary scan feature of Sunter to Volk et al., in order to provide additional specialized testing.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Volk et al., U.S. Patent No. 4792950 as applied to claim 1 above, and further in view of Gotoh et al., U.S. Patent Application 2003/0046015. Volk et al fails to teach the input circuit as claimed in claim 1, wherein the input circuit is configured to be switched off. But Gotoh et al. does teach this feature in FIG.10, where the input circuit 220 is switched off by circuit 240, when the circuit is not in test mode. And in column 3 paragraph [0021], the

inventor cites the advantage of a circuit that can test and provide verification of inputs without degrading circuit performance (column 2 paragraph [0012]. One with ordinary skill in the art at the time of the invention, motivated as suggested, would find it obvious to include the separate BSC circuit of Gotoh et al. in order to improve the performance of a differential receiver.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

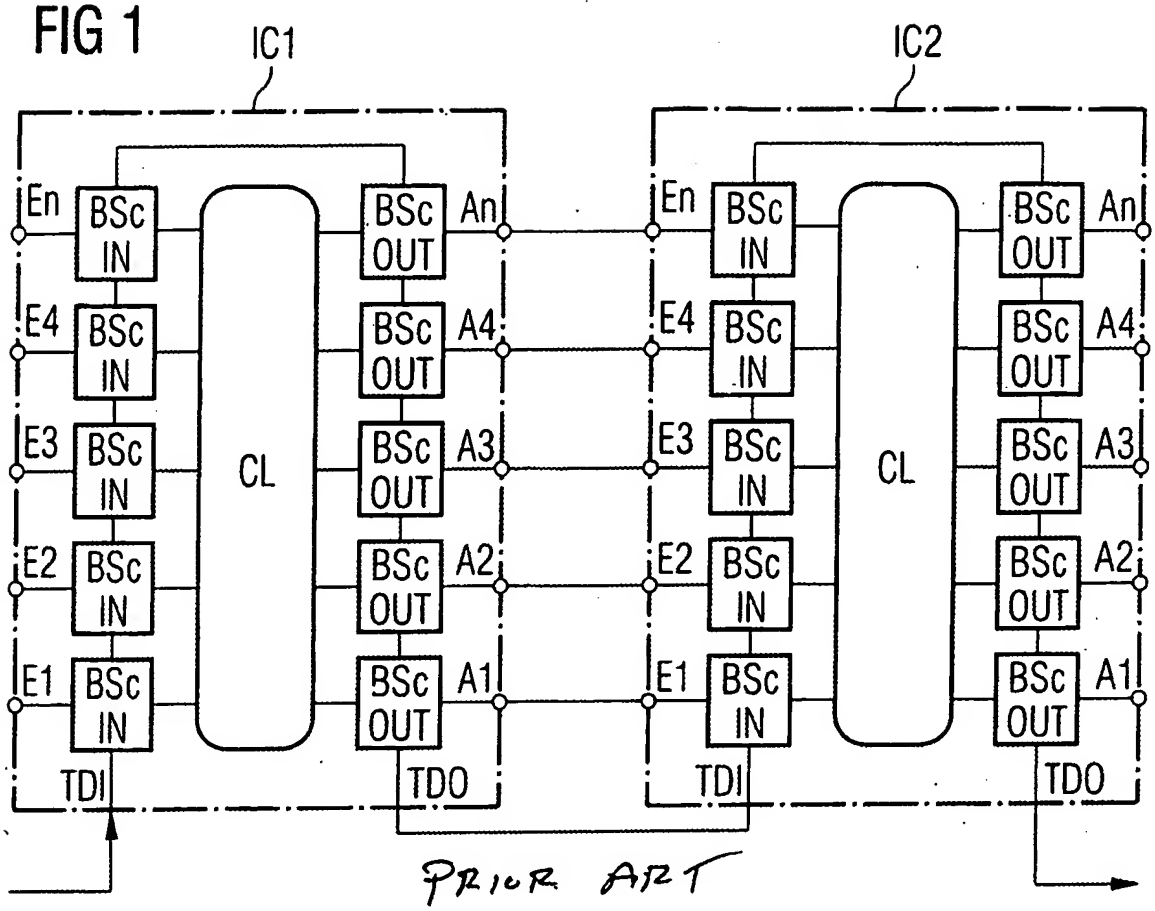
GUY LAMARRE
PRIMARY EXAMINER

Changes Approved 4/20/05 MPL

NOV 2 4 2004
PATENT & TRADEMARK OFFICE

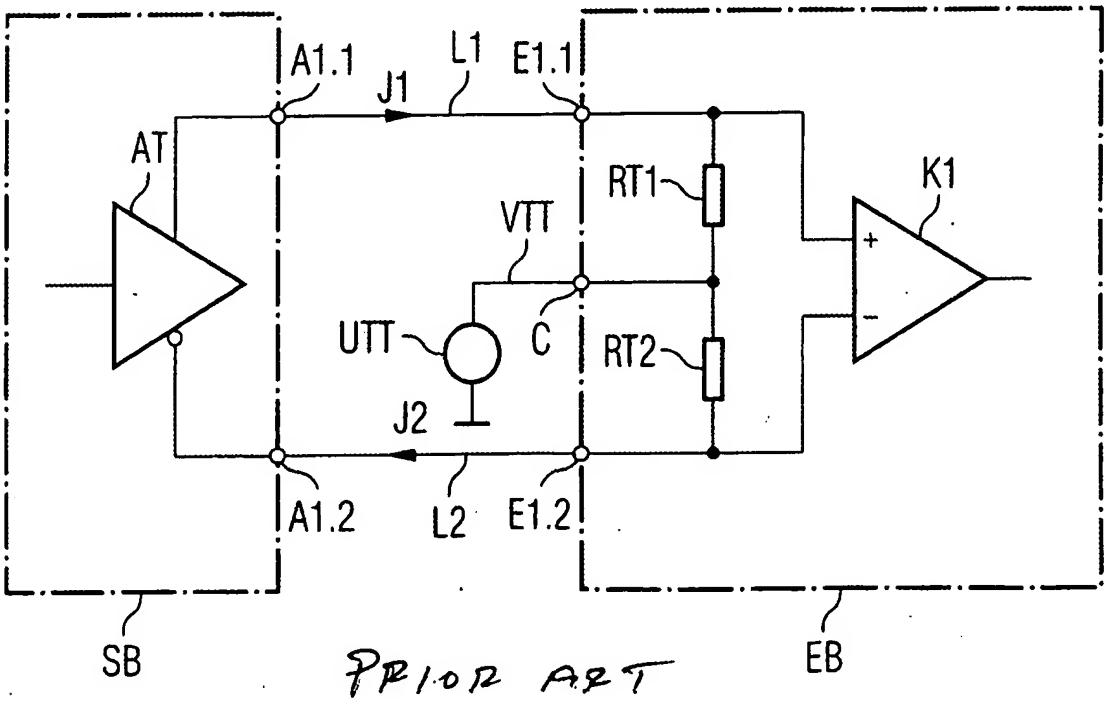
REPLACEMENT SHEET

FIG 1



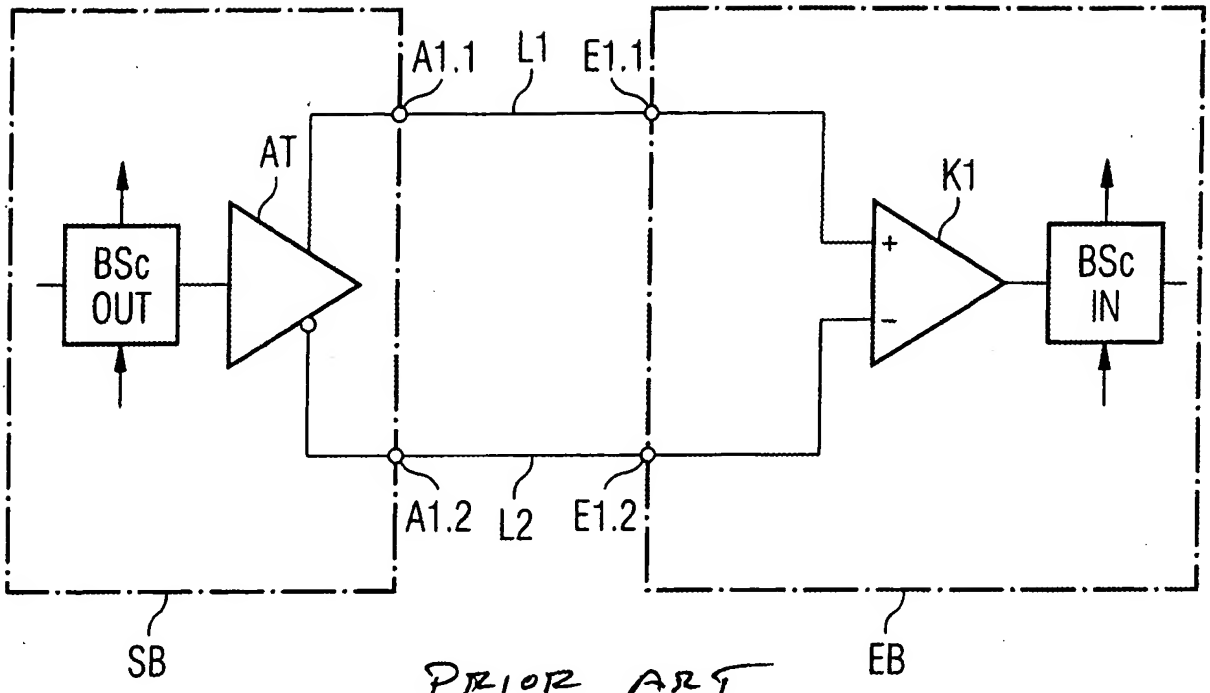
PRIOR ART

FIG 2



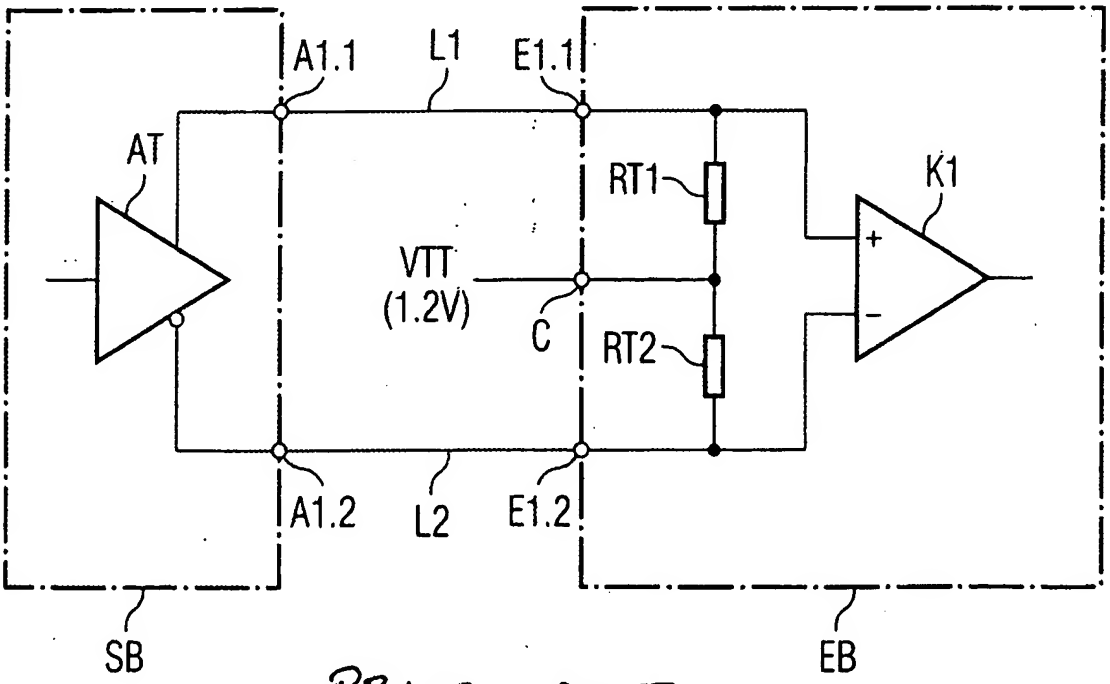
PRIOR ART

FIG 3



PRIOR ART

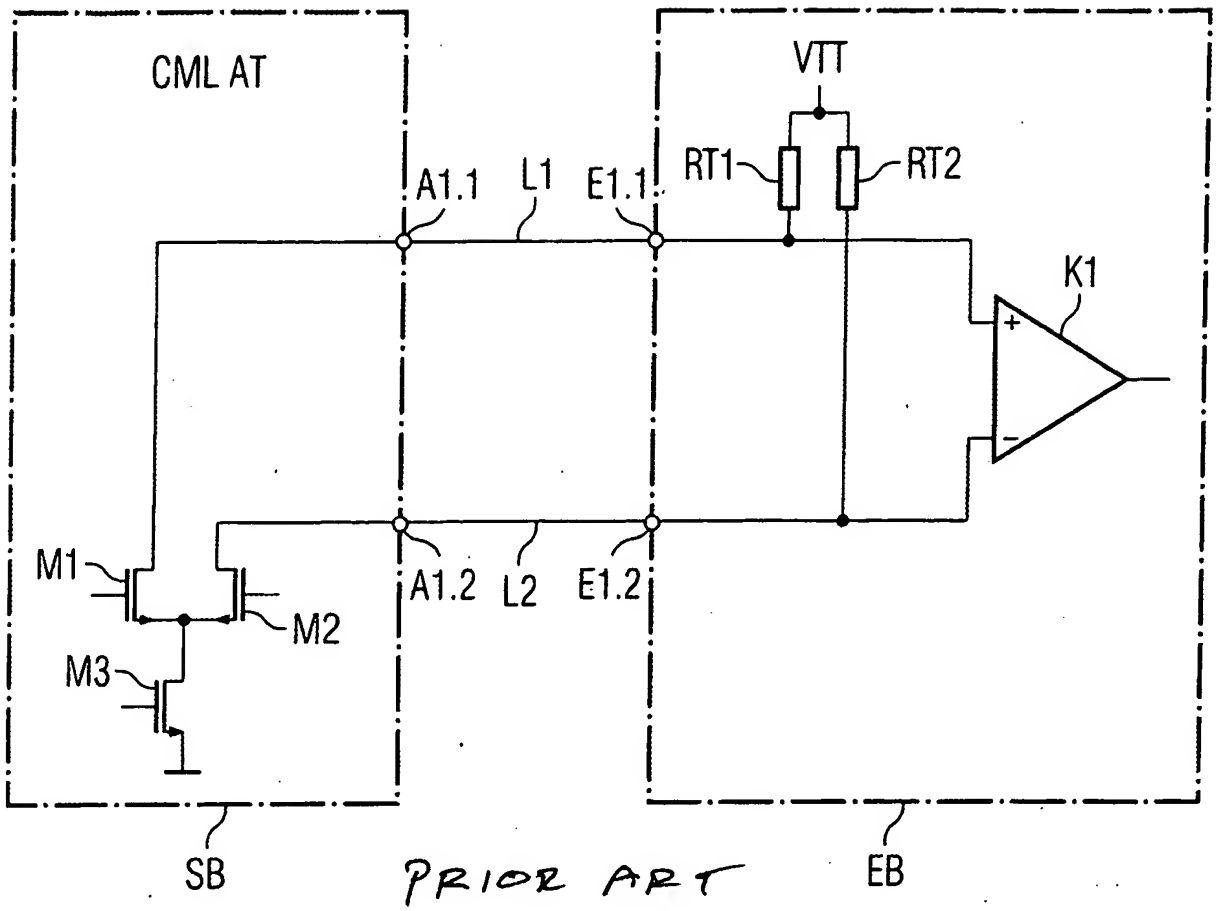
FIG 4



PRIOR ART

AMENDED

FIG 5



PRIOR ART

ANNOTATED

FIG 6